REMARKS

Applicant has carefully reviewed this Application in light of the Office Action mailed November 15, 2005. Claims 1 and 3-5 are pending in this Application. Claims 2, 6 and 7 were previously cancelled without prejudice or disclaimer. Claims 1 and 3-5 stand rejected under 35 U.S.C. § 102(b). Claim 1 has been amended to further define various features of Applicants invention. Applicant respectfully requests reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 102

Claims 1 and 3-5 were rejected by the Examiner under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,945,507 issued to Ryuji Ishida et al ("Ishida"). Applicant respectfully traverses and submits the cited art does not teach all of the elements of the claimed embodiment of the invention.

Ishida discloses an overflow correction circuit for use in an arithmetic operation circuit. Specifically, Ishida discloses an adder 10 whose output 22 can be detected for an overflow condition by detector 34. Depending upon the type of overflow condition, overflow detector 34 then directs the selector to forward one of three values (the maximum value 28, the minimum value 32 or the results of the adder 10) to the accumulator 46.

Claim 1 recites a system comprising "an accumulator, operatively connected to store at least a portion of the result of the added operands or at least a portion of a selected one of pre-determined constants based on control signals" and "guard bits, operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals."

Applicant respectfully submits that the cited reference fails to disclose each and every element of Applicant's invention. For example, Ishida fails to teach a system for overflow and saturation processing comprising "guard bits, operatively connected to store the *remaining portion* of the result of the added operands or the *remaining portion* of the selected one of predetermined constants based on the control signals," as recited by amended Claim 1.

Ishida teaches a method and system for detecting and correcting overflow in an arithmetic circuit (*see* Abstract) but does not store the result of the overflow. On the other

hand, the present invention contemplates, *inter alia*, not only detection of overflow (*e.g.* overflow logic), but also stores overflow (*e.g.* guard bits), and detects whether such overflow itself overflows (*e.g.* saturation logic). As further illustration, Ishida teaches an accumulator 46 that stores the *entire* 24-bit result of adder 10 or an entire pre-determined constant 28 or 32. (*See* Fig. 1). Hence, assuming *arguendo* that another element of the circuit disclosed by Ishida can even be considered "guard bits" as contemplated by the present invention, no such element can hold "the remaining portion of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals" as recited in amended Claim 1. Since Ishida's accumulator stores the *entire* result of an adder (See Fig. 1, adder 10 is a 24-bit adder and accumulator 46 is a 24-bit accumulator), it is logically impossible that there exists a "remaining portion" of the result that is not stored in the accumulator, as contemplated in Claim 1.

For at least these reasons, the cited reference fails to disclose the recited elements and therefore, cannot anticipate Claim 1. Given that Claims 3-5 depend from Claim 1, Applicant respectfully submits that Claims 3-5 are allowable. As such, Applicant respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. § 102(b) and allow Claims 1 and 3-5.

Rejections under 35 U.S.C. § 132(a)

The Examiner has objected to the Amendment filed September 6, 2005 under 35 U.S.C. § 132(a) because it introduces new matter into the disclosure and is not fully persuasive. Applicant has amended Claim 1 without prejudice or disclaimer in order to overcome this objection.

Information Disclosure Statement

Applicant encloses an Information Disclosure Statement and PTO Form 1449, with a copy of the reference for the Examiner's review and consideration.

CONCLUSION

Applicant appreciates the Examiner's careful review of the Application. Applicant has now made an earnest effort to place this case in condition for allowance in light of the amendments and remarks set forth above. Applicant respectfully requests reconsideration of the rejections and full allowance of Claims 1 and 3-5 as amended.

Applicant believes there are no fees due at this time, however, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-2148 of Baker Botts L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicant's attorney at 512.322.2581.

Respectfully submitted,
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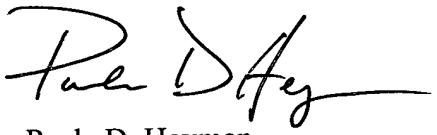

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